MPE720 Ver.7.97 Version Up Information

1. Functional Additions and Improvements

1.1 Ver.7.97 Version Up Information

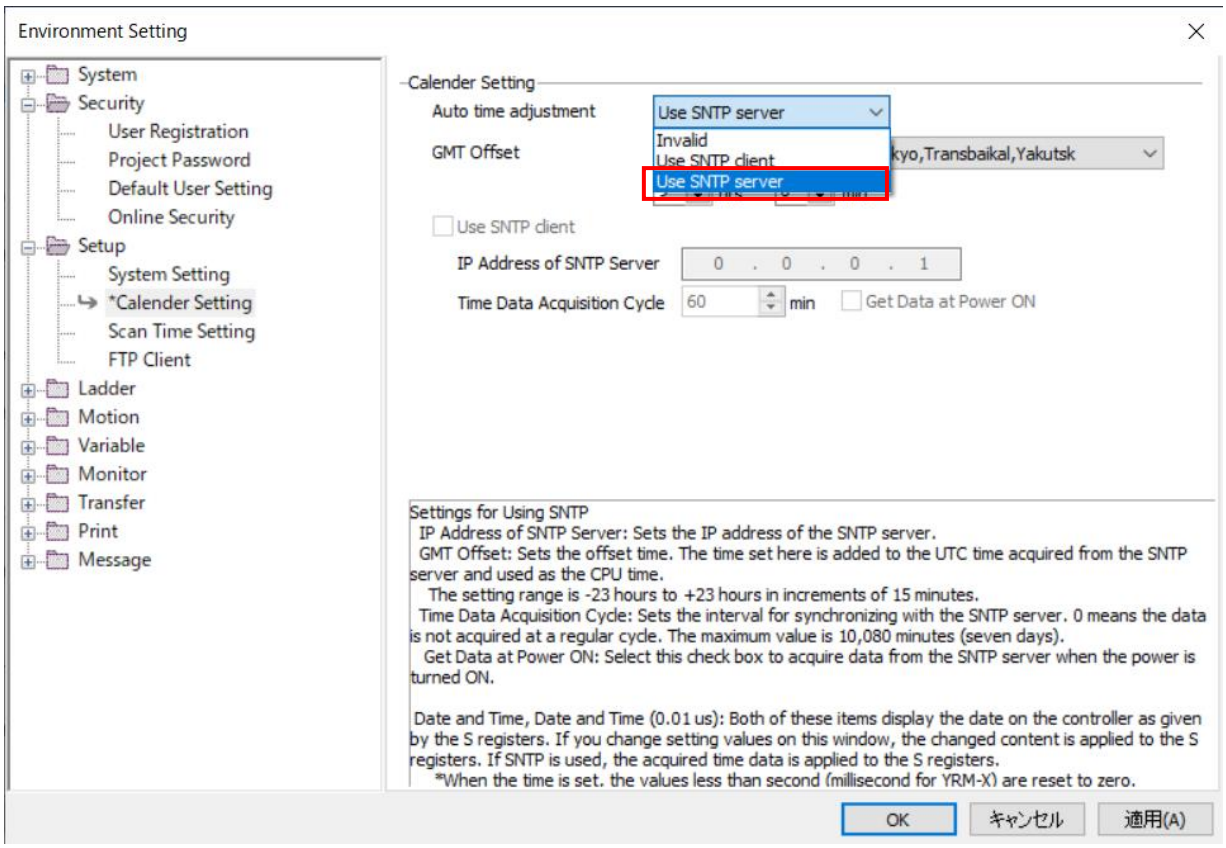
Items added and features improved from MPE720 Ver.7.96 to Ver.7.97 are as follows:

No.	Function items	classification
1.	SNTP server function is now supported.	New Function
2.	MPX1312-2 Added support for 3 optional slot base unit.	Function Enhancement
3.	From CPU-203/CPU-203F (including sub-CPUs) to YRM1000 series models and MPX1000 series models Project conversion is now supported.	Function Enhancement
4.	I/O Unit Parameter Read/Write System Function Instructions have been added.	Function Enhancement
5.	Several bugs have been fixed.	Improvement

2. Details of the amendment

No. 1 SNTP server function is now supported.

In Calendar Settings, "Use SNTP Server" can be selected as a time synchronization adjustment.
With this function, time synchronization can be performed with subordinate controllers that have an SNTP client function.



The models that support the SNTP server function in this version are as follows.

series	model	Supported Firmware Versions
YRM1000	CPU-12	2.07

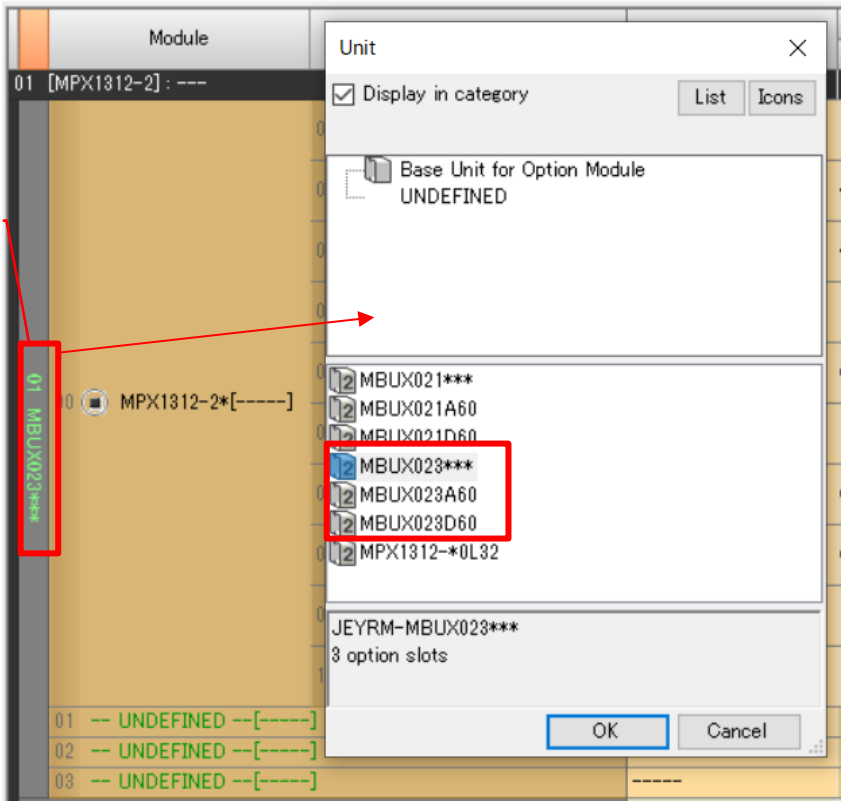
No. 2　MPX1312-2 Added support for 3 optional slot base units.

In the module configuration definition, you can configure the base unit of the MPX1312-2 with three option slots. There are three types of base units that can be selected.

■ 3 Optional Slot Base Unit

- MBUX023A60 (Power supply type: AC100/200V Input 60W)
- MBUX023D60 (Power supply type: DC24V Input 60W)
- MBUX023*** (Power supply type: not specified)

Click on the base unit name,
Base unit can be changed.



[Supported versions]

model	Supported Firmware Versions
MPX1312-2	2.08

No. 3　Added support for project conversion from CPU-203/CPU-203F (including sub-CPUs) to YRM1000 series and MPX1000 series models.

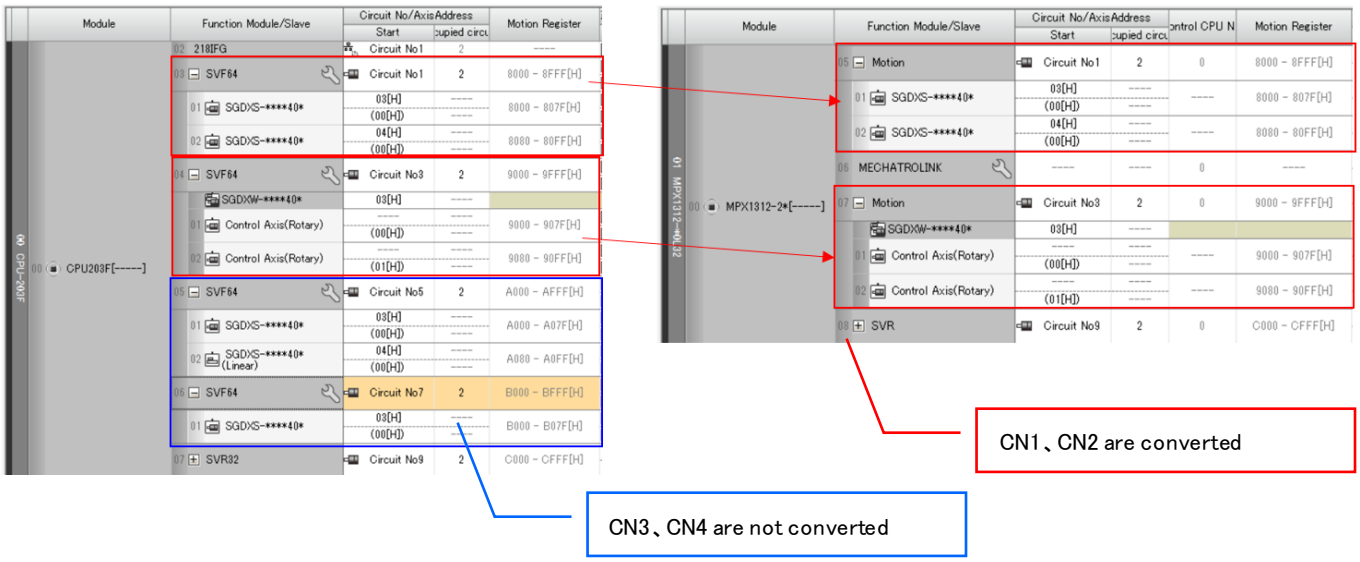
1）The following combinations of project conversions are now supported. (The same applies when the conversion source is a sub-CPU.)

Convert from	Convert to
CPU-203（SUB）	CPU-01
CPU-203（SUB）	CPU-12
CPU-203（SUB）	MPX1312-2
CPU-203（SUB）	MPX1012J
CPU-203F（SUB）	CPU-01
CPU-203F（SUB）	CPU-12
CPU-203F（SUB）	MPX1312-2
CPU-203F（SUB）	MPX1012J

2）The SVC64 integrates all allocation slaves of CN1, CN2, CN3, and CN4, as well as the conversion of the CPU-203 → MP3000 series models.
Assign to the built-in Motion module.

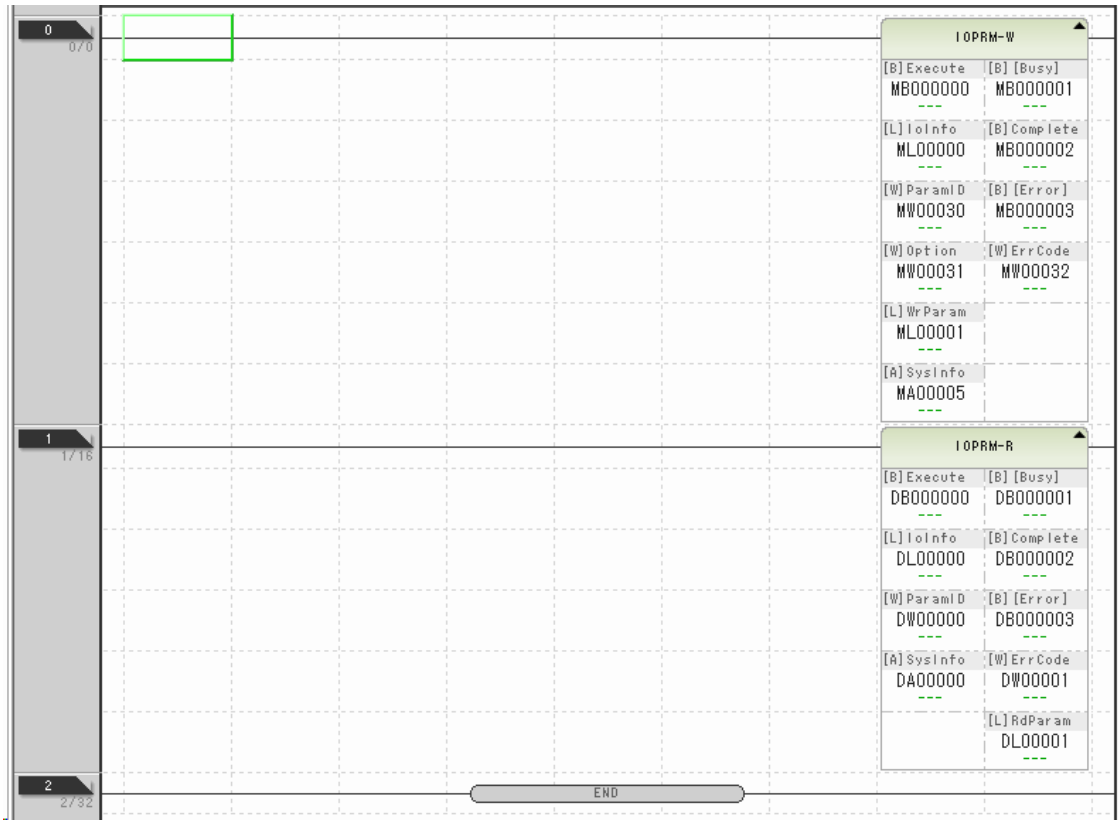
3）In SVF64, CN1 and CN2 are assigned to the built-in Motion module of the conversion destination. CN3 and CN4 are not converted. Also, if the destination has only one built-in Motion module, CN2 will not be converted either.

Example: When converting to CPU-203F → MPX1312-2



No. 4 I/O Unit Parameter Read/Write System Function Instruction has been added.

IOPRM-W (to write the parameters of the IO unit) and IOPRM-R (to read the parameters of the IO unit) have been added to the system functions of the ladder program.



The models that are compatible with this instruction are as follows.

series	model	Supported Firmware Versions
YRM1000	CPU-12	2.07
MPX1000	MPX1312-2	

No. 5 Several bugs have been fixed.

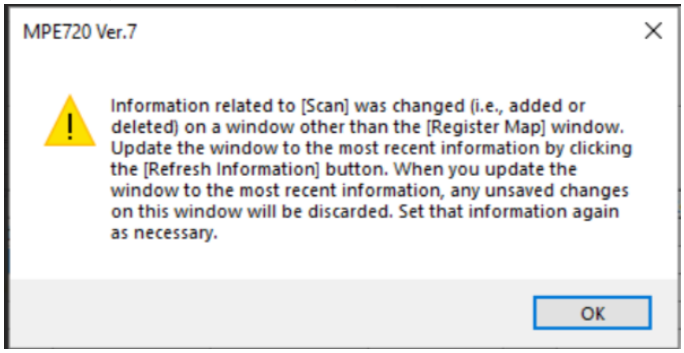
1) When "Search in project" or "Replace in project" is executed on a multi-scan model, corrected the notation of the scan name of the message that is displayed in the output window.

Before Modification	After the fix
Scan20	Start
Scan30	Interrupt
Scan0	H
Scan1	L

2) Fixed a bug that caused the MPE720 to freeze when the option unit 262IF-01 (FL-net communication module) was assigned in the module configuration definition, the detailed setting screen was opened, and the settings were saved.

3) Fixed a bug that when compiling the EXPRESSION, IF, and WHILE instructions of a Start drawing or Interrupt drawing when the "Support Access Control between scans" setting is set to "Enabled" on a multi-scan model, a warning of "Out of register setting range" or "A motion register of an unassigned axis is being used" is displayed.
Compile warnings are not detected for Start drawings and Interrupt drawings due to Support Access Control between scans.
Start drawings and Interrupt drawings are not subject to compilation warning detection due to Support Access Control between scans.

4) After exporting with Register Map, if you continue to edit the Register Map and then save, the following fixed a bug that prevented saving due to an error message.



Appendix A: Compilation of Parallel Circuits

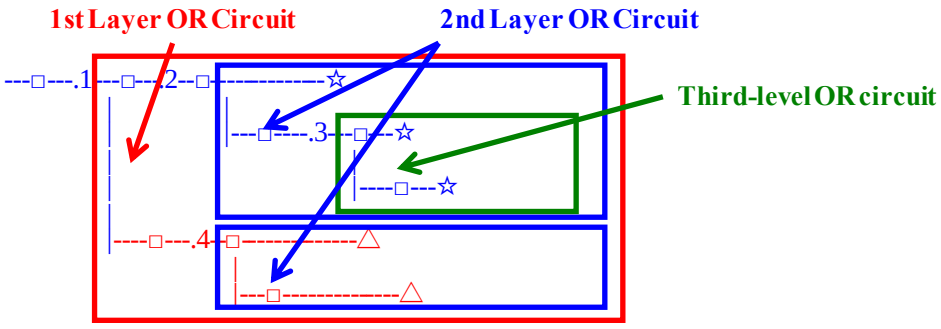
In the ladder program of MPE720 Ver7.23 or earlier, the following symptoms may occur when using parallel circuits.

< phenomenon>

When a circuit containing the following pattern was created, there was a phenomenon that the circuit on the lower side of the first-layer OR circuit originally received a conditional instruction in front of the first-level OR circuit and operated without being subjected to the condition.

< measures>

If this phenomenon occurs, recompile the corresponding ladder program with MPE720 Ver7.24 or later MPE720 Ver7. Alternatively, select "Compile All Program" from the "Compile" menu again.



1st level OR circuit: OR circuit branched from Lang's busbar
2nd layer OR circuit: OR circuit branched from within the 1st level OR circuit
3rd level OR circuit: OR circuit branched from within the 2nd level OR circuit

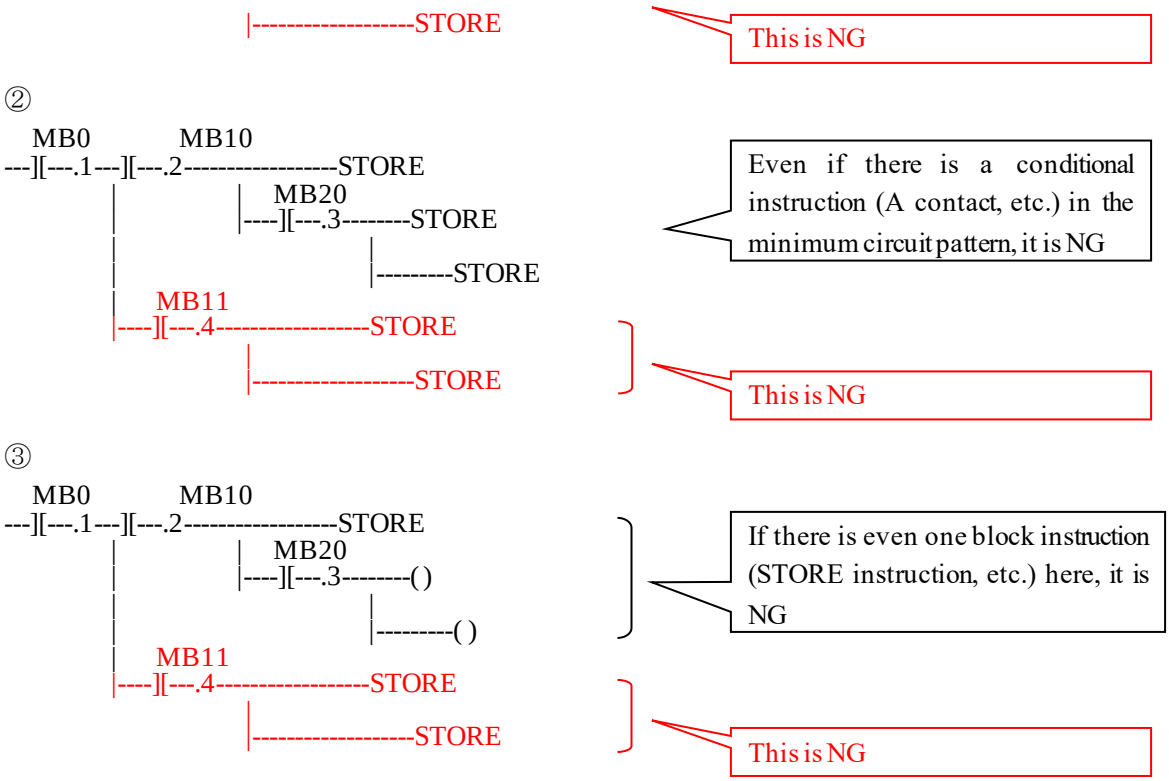
☐ (Conditional Instructions): A contact, B contact, comparison (==, !=, >, <) instructions, etc.
* ☐ (conditional instructions) includes power wires (−−−−−−)
☆ (Output instructions): coils, block instructions (Expression, STORE, COPYW) instructions, etc.
* However, if all ☆ are coil instructions, this phenomenon will not occur.
△ (Output instructions): Coils, block instructions (Expression, STORE, COPYW) instructions, etc.

[Phenomenon occurrence pattern]

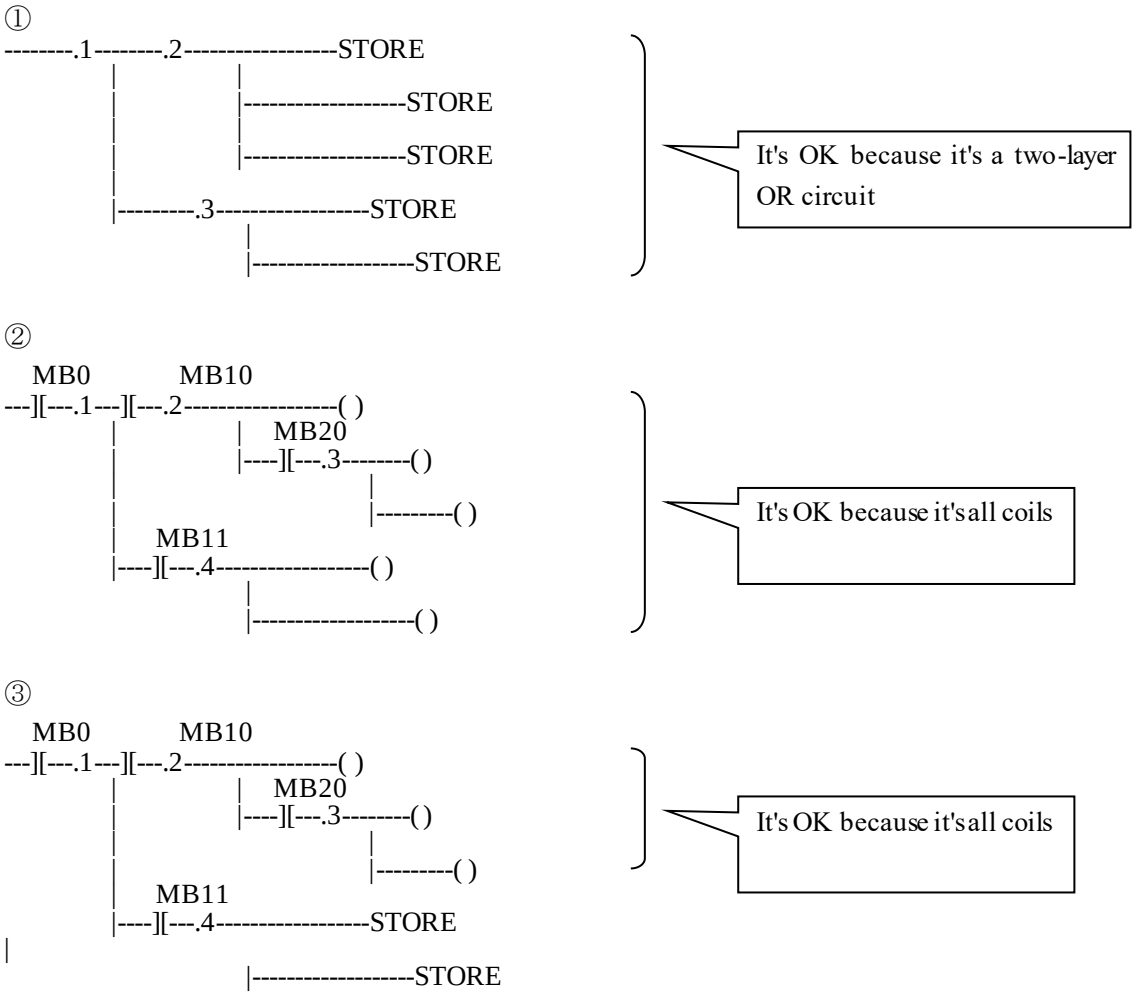
symbol	order
][	A contact
STORE	STORE command
( )	coil

[NG pattern]

①


|----------STORE
This is NG
②
MB0
MB10
---][---.1---][---.2----------STORE
MB20
|----][---.3--------STORE
|---------STORE
MB11
|----][---.4----------STORE
|----------STORE
Even if there is a conditional instruction (A contact, etc.) in the minimum circuit pattern, it is NG
This is NG
③
MB0
MB10
---][---.1---][---.2----------STORE
MB20
|----][---.3--------( )
|---------( )
MB11
|----][---.4----------STORE
|----------STORE
If there is even one block instruction (STORE instruction, etc.) here, it is NG
This is NG

[OK pattern]

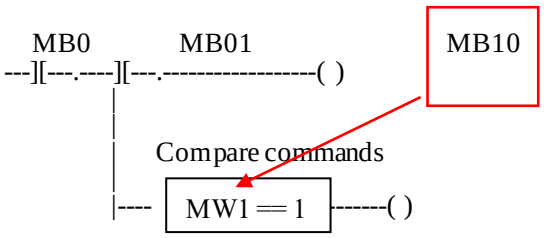

①
--------.1--------.2----------STORE
|----------STORE
|----------STORE
|---------.3----------STORE
|----------STORE
It's OK because it's a two-layer OR circuit
②
MB0
MB10
---][---.1---][---.2----------( )
MB20
|----][---.3--------( )
|---------( )
MB11
|----][---.4----------( )
|----------( )
It's OK because it'sall coils
③
MB0
MB10
---][---.1---][---.2----------( )
MB20
|----][---.3--------( )
|---------( )
MB11
|----][---.4----------STORE
|
|----------STORE
It's OK because it'sall coils

Appendix B: Compilation when there are comparison instructions in a parallel circuit

MPE720 Ver7.In the ladder program of the MPE720 Ver7 before 63, the following symptoms may occur when using parallel circuits.

< phenomenon >

When a circuit containing the following pattern was created, the value of the register set in the upper circuit of the OR circuit was reflected in the next scan when it should have been reflected in the comparison instruction in the subsequent OR circuit in the same scan.



A pattern in which a register set in the circuit above the parallel circuit is referenced in subsequent comparison instructions in the parallel circuit.

< measures>

If this phenomenon occurs, recompile the corresponding ladder program with MPE720 Ver7.64 or later MPE720 Ver7. In addition, the number of internal steps changes in programs that include circuits with this pattern in Ver. 7.64 or later, so there is a possibility that you may jump to an unintended place when cross-referencing is performed in a project created in the previous version. In that case, please recompile the program. Alternatively, select "Compile All Program" from the "Compile" menu again.

Appendix C: High DPI

When the MPE720 Ver.7 was started on a computer that supports high DPI, such as a 4K display, part of the screen could not be displayed depending on the resolution and scale settings. Therefore, from MPE720 Ver.7.67, the high DPI setting of the MPE720 properties has been disabled. This avoids phenomena such as screen cutouts. If you need to use it at a high DPI setting due to circumstance